



HiDFT®-SIGNOFF

RTL Testability Debug & Signoff

DATASHEET

Overview

HiDFT-SIGNOFF allows designers to create a high-level design for test signoff methodology, closing the gap between RTL and DFT. HiDFT-SIGNOFF allows early identification of test issues and enables new pre-synthesis design and DFT verifications. HiDFT-SIGNOFF is the unique EDA tool that allows scan logic insertion at RTL.

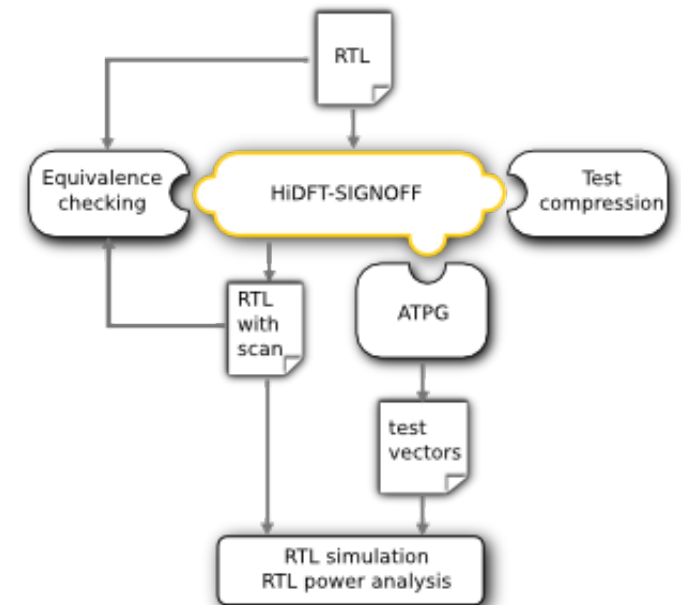
Key Features

- Enables testability signoff
- Testability DRC
- ATPG-aware Test Coverage Evaluation (TCE)
- Accuracy of Test Coverage Evaluation (TCE) within 0.5%
- AutoFix correction of scannability problems
- Pinpoints testability weaknesses (controllability / observability issues)
- Test point insertion for test coverage improvement
- Hierarchical scan insertion methodology using test models (CTL)
- Graphical interface to debug ATPG faults
- Allows new DFT verifications at RTL : test vectors simulation, test power analysis, etc...

Key Benefits

- Speed-up the test coverage enhancement process
- Speed-up simulation & test power analysis
- Get accurate test coverage evaluation at RTL
- Debug RTL in correlation with the ATPG process

Methodology



Headquartered in Moirans (Grenoble area, France), DeFacto Technologies is an innovative chip design software company developing breakthrough technology to dramatically enhance the DFT process and increase the testability of integrated circuits (ICs) and systems on a chip (SoCs).

Our mission is to enable designers to complete planning, analysis and insertion of integrated circuit test logic before synthesis by delivering a high quality suite of tools working at the register transfer level (RTL).

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